**IN THE UNI1450TED STATES PATENT AND TRADEMARK OFFICE**

Applicant(s): Takahiko KISHI

Examiner: Eva Y. ZHENG

Serial No.: 09/931,124

Group Art Unit: 2611

Filed: August 16, 2001

Docket: 678-724 (P9876)

For: **DIGITAL DOWN-CONVERTER AND RECEIVER**

Dated: December 26, 2006

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

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Respectfully submitted,

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Dated: December 26, 2006

Michael J. Musella

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

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## APPEAL BRIEF

### REAL PARTY IN INTEREST

The real party in interest is Samsung Electronics Co, Ltd, the assignee of the subject application, having an office at 416, Maetan-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do, Republic of Korea.

### RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge and belief, there are no currently pending related appeals, interferences or judicial proceedings.



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Dated: December 26, 2006

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## STATUS OF CLAIMS

Original Claims 1-8 were filed on August 16, 2001. Claims 1, 3 and 4 were amended, and new Claims 9-19 were added in an Amendment filed February 25, 2005. Claims 1, 5 and 14-16 were amended in an Amendment filed September 28, 2005. Claims 1, 5, 7-16 and 18 were amended, and Claim 19 was cancelled in an Amendment filed April 10, 2006. Thus, Claims 1-18 are pending in the Appeal. Claims 1, 5 and 16 are in independent form. For the purposes of this appeal, Claims 1-4 and 9-15 stand or fall together, Claims 5-8 stand or fall together, and Claims 16-18 stand or fall together.

## STATUS OF AMENDMENTS

An Office Action marked "Final" was mailed on June 23, 2006. A Request for Reconsideration, which did not contain any claim amendments, was filed on September 22, 2006. An Advisory Action issued on October 13, 2006.[1]

## SUMMARY OF CLAIMED SUBJECT MATTER

The invention as recited in Claim 1 relates to digital down-converter for converting a frequency of a digital signal, received at a radio receiver and sampled with a radio frequency (RF) or an intermediate frequency (IF), to a detection frequency for a detection process.

The digital down-converter 307 contains a first mixer 201 for converting and outputting a frequency of the digital signal to a frequency of a first IF signal by multiplying the digital signal by a real signal. Specification, page 6, line 12 – page 9, line 3.

The digital down-converter 307 also contains a decimation filter 203 for suppressing unwanted components among the frequency of the first IF signal from the first mixer 201. Specification, page 6, line 12 – page 9, line 3.

1 It is duly noted that the Advisory Action states in paragraph 7 thereof "the proposed amendments... will not be entered". No amendments were proposed at the time of the issuance of the Advisory Action. All amendments to date have been entered by the Examiner. This error is respectfully brought to the attention of the Board of Patent Appeals and Interferences ("the Board").

The digital down-converter 307 also contains a second mixer 205 for converting the frequency of the first IF signal having only wanted components outputted by the decimation filter 203 to a second IF signal of the detection frequency, and outputting the second IF signal as a complex signal by multiplying the output of the decimation filter 203 by a complex local signal. Specification, page 6, line 12 – page 9, line 3.

The second mixer 205 of the apparatus contains a first selector 205a for cyclically selecting a multiplication value among cosine wave values of the local signal. Specification, page 6, line 12 – page 9, line 3.

The second mixer 205 of the apparatus also contains a second selector 205b for cyclically selecting a multiplication value among sine wave values of the local signal. Specification, page 6, line 12 – page 9, line 3.

The invention as recited in Claim 5 relates to a receiver.

The receiver contains a digital down-converter 307 including a first mixer 201 for converting a frequency of a received digital signal, sampled with a radio frequency (RF) or an intermediate frequency (IF), to a frequency of a first IF signal by multiplying the digital signal by a real signal, and a second mixer 205 for converting the first IF signal converted by the first mixer 201 to a second IF signal of a detection frequency for a detection process and then outputting the second IF signal as a complex signal by multiplying the first IF signal by a complex local signal. Specification, page 6, line 12 – page 9, line 3.

The receiver also contains an RF unit 302 for receiving an input signal and providing the received signal to the digital down-converter 307 for frequency conversion. Specification, page 6, line 12 – page 9, line 3.

The receiver also contains a filter 305 for attenuating an aliasing frequency component and an image frequency component of the first mixer 201 in the digital down-converter 307, from an output of the radio receiver. Specification, page 6, line 12 – page 9, line 3.

The receiver also contains an analog-to-digital converter 306 for sampling an output of the filter 305 with a radio frequency or an intermediate frequency and providing the sampled signal to the digital down-converter 307. Specification, page 6, line 12 – page 9, line 3.

The second mixer 205 contains a first selector 205a for cyclically selecting a multiplication value among cosine wave values of the local signal. Specification, page 6, line 12 – page 9, line 3.

The second mixer 205 also contains a second selector 205b for cyclically selecting a multiplication value among sine wave values of the local signal. Specification, page 6, line 12 – page 9, line 3.

The invention as recited in Claim 16 relates to a digital down-converter 307 for converting a frequency of a digital signal, received at a radio receiver and sampled with a radio frequency (RF) or an intermediated frequency (IF), to a detection frequency for a detection process.

The digital down-converter 307 contains a first mixer 201 for converting and outputting a frequency of the received signal to a frequency of a first IF signal by multiplying the digital signal by a real signal. Specification, page 12, line 1 – page 14, line 24.

The digital down-converter 307 also contains a second mixer 211 for dividing the frequency of the first IF signal into a cosine part and a sine part and processing the cosine part and the sine part with a polyphase structure for converting and decoding to the frequency of a second IF signal by multiplying the first IF signal by a complex local signal. Specification, page 12, line 1 – page 14, line 24.

The second mixer 211 contains a selector 212a or 212b for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals. Specification, page 12, line 1 – page 14, line 24.

## GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

Whether Claims 5-8 under 35 U.S.C. §112, second paragraph, are indefinite.

Whether Claims 1, 5 and 16 under 35 U.S.C. §103(a) are unpatentable over U.S. Patent 5,375,146 (Chalmers) in view of U.S. Patent 6,697,603 (Lovinggood et al.), and further in view of U.S. patent 5,696796 (Poklemba).

Whether Claims 2-4, 6-15, 17 and 18 under 35 U.S.C. §103(a) are unpatentable over U.S. Patent 5,375,146 (Chalmers) in view of U.S. Patent 6,697,603 (Lovinggood et al.), and further in view of U.S. patent 5,696796 (Poklemba), and further in view of U.S. Patent 6,061,385 (Ostman).

## ARGUMENT

1. Claim 5-8 particularly point out and distinctly claim the subject matter which the applicant regards as his invention

The Examiner rejected Claims 5-8 under 35 U.S.C. §112, second paragraph, as being indefinite. Regarding the rejection of Claim 5 under §112, second paragraph, the Examiner stated on page 2 of the June 2006 Office Action that the claim is "unclear and confusing." Specifically, the Examiner stated:

> Regarding to claim 5, claimed subject matter is unclear and confusing. It seems like claim 5 is regarding to embodiment of Fig. 2. The BPF 305 is output to ADC 306. If the filter in claim indicates as BPF 305, then it is not relate to the first mixer in the digital down-converter. On the other hand, if the claimed filter-is decimation filter of Fig. 1, then it is not input to ADC. [Errors in original.]

Claim 5 recites, "a filter for attenuating an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter, from an output of the radio receiver". Thus the filter attenuates a signal output from the radio receiver. The aliasing frequency component and the image frequency component are attenuated from the signal. The attenuation of the aliasing frequency component and the image frequency component is based on the first mixer characteristics. This is clearly set forth in the Specification at page 9, lines 10-21, and at page 10, lines 15-22. Claim 5 is clear and concise.

In addition, in Claim 5 of the present application, the filter is the BPF 305. Referring to the explanation of the BPF 305 in the detailed description of the present application, "the BPF 305 is an analog filter arranged in front of an A/D converter 306, which can suppress an interference signal of an image frequency inputted to a DDC" and "an analog filter 305 only needs to suppress the interference signal of an aliasing frequency and the image frequency". Hence, Claim 5 is clear and concise.

The Examiner has failed to show that Claims 5-8 are indefinite. The Examiner has failed to make out a prima facia case for an indefinite rejection.

Claims 5-8 particularly point out and distinctly claim the subject matter which the applicant regards as his invention, and thus the rejection under §112, second paragraph, of Claims 5-8 must be reversed.

2. Independent Claims 1, 5 and 16 are patentable over Chalmers in view of Lovinggood et al., and further in view of Poklemba

Independent Claims 1, 5, and 16 were said to be unpatentable over Chalmers in view of Lovinggood et al., and further in view of Poklemba.

2.A. The digital down converter of Claim 1 is patentable over Chalmers in view of Lovinggood et al., and further in view of Poklemba

Claim 1 recites a digital down converter for converting a frequency of a digital signal, received at a radio receiver and sampled with a radio frequency (RF) or an intermediate frequency (IF), to a detection frequency for a detection process, that includes a first mixer for converting and outputting a frequency of the digital signal to a frequency of a first IF signal by multiplying the digital signal by a real signal; a decimation filter for suppressing unwanted components among the frequency of the first IF signal from the first mixer; and a second mixer for converting the frequency of the first IF signal having only wanted components outputted by the decimation filter to a second IF signal of the detection frequency, and outputting the second IF signal as a complex signal by multiplying the output of the decimation filter by a complex local signal; the second mixer includes a first selector for cyclically selecting a multiplication value among cosine wave values of the local signal, and a second selector for cyclically selecting a multiplication value among sine wave values of the local signal.

2.A.1. The decimation filter for suppressing unwanted components among the frequency of the first IF signal from the first mixer is not inherent in Chalmers

The Examiner on page 3, lines 11-13 of the June 2006 Office Action states that the decimation filter for suppressing unwanted components among the frequency of the first IF signal

from the first mixer is inherent in and disclosed by Chalmers, and cites col. 1, lines 49-51. The cited section of Chalmers states, "Variations employing different numbers of conversion stages also are known. In any event, each such conversion stage requires a mixer, an LO, and a filter to remove the undesired mixer products."

It is well settled "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

Since a decimation filter is a finite impulse response filter with specific characteristics, an inherency argument is not only misplaced but also improper.

The decimation filter recited in Claim 1 is not inherent in Chalmers. Lovinggood et al. and/or Poklemba do not cure these defects.

2.A.2. <u>The second mixer as recited in Claim 1 is not taught or disclosed by Chalmers</u>

Claim 1 recites a second mixer for converting the frequency of the first IF signal having only wanted components outputted by the decimation filter to a second IF signal of the detection frequency. The Examiner equates this feature of Claim 1 with mixer 112 of Chalmers. The second mixer of Claim 1 receives the signal output from the decimation filter. Chalmers in FIG. 1 illustrates its mixer 112 receiving a signal from amplifier 110.

Claim 1 further recites that the second mixer outputting the second IF signal as a complex signal by multiplying the output of the decimation filter by a complex local signal. The Examiner now equates the second mixer of Claim 1 with mixer 132 illustrated in FIG. 1 of Chalmers. The Examiner has thus far equated the second mixer of Claim 1 with both mixer 112 and mixer 132 of FIG. 1 of Chalmers. Further, this feature of Claim 1 states that the second mixer multiplies the output of the decimation filter by a complex local signal. Neither mixer 112 nor mixer 132 of Chalmers multiplies the output of the decimation filter by a complex local signal.

The second mixer of Claim 1 is not taught or disclosed by Chalmers; Lovinggood et al. and/or Poklemba do not cure these defects.

2.A.3. The first and second selectors of Claim 1 are not taught or disclosed by Chalmers and/or Poklemba

Claim 1 still further recites that the second mixer comprises a first selector for cyclically selecting a multiplication value among cosine wave values of the local signal, and a second selector for cyclically selecting a multiplication value among sine wave values of the local signal. The Examiner opines that Poklemba discloses these features, and specifically points to the normal/inverting gating circuits (106 and 108) and multiplexer (110) of FIG. 4. The normal/inverting gating circuits 106 and 108 are not selectors as recited in Claim 1 and defined in the specification.

The first and second selectors of Claim 1 are not taught or disclosed by Chalmers and/or Poklemba; Lovinggood et al. does not cure these defects.

2.A.4. The second mixer for converting the frequency of the first IF signal having only wanted components output by the decimation filter to a second IF signal of the detection frequency, and outputting the second IF signal as a complex signal by multiplying the output of the decimation filter by a complex local signal of Claim 1 is distinguishable from the filter of Chalmers in view of Lovinggood et al., and further in view of Poklemba

A second mixer for converting the frequency of the first IF signal having only wanted components outputted by the decimation filter to a second IF signal of the detection frequency, and outputting the second IF signal as a complex signal by multiplying the output of the decimation filter by a complex local signal of the present application are distinguishable from a filter to remove products of an undesired mixer products and a mixer 112 of Chalmers.

The Examiner alleged that a first selector and a second selector of a second mixer in the present application are equivalent to a NORM/INVERT (106, 108) of Poklemba. However, Poklemba merely recites that the NORM/INVERT (106, 108) outputs (+1, 0, -1, 0) of a cosine sample and (0, +1, 0, -1) of a sine sample, and multiplies an I channel and a Q channel using the above sample values. Chalmers and Poklemba do not teach or disclose how the filter of Chalmers could be combined with the NORM/INVERT (106, 108) of Poklemba to produce a second mixer for converting the frequency of the first IF signal having only wanted components outputted by the decimation filter to a second IF signal of the detection frequency, and outputting the second IF signal

as a complex signal by multiplying the output of the decimation filter by a complex local signal of Claim 1.

The second mixer for converting the frequency of the first IF signal having only wanted components outputted by the decimation filter to a second IF signal of the detection frequency, and outputting the second IF signal as a complex signal by multiplying the output of the decimation filter by a complex local signal of Claim 1 are not taught or disclosed by Chalmers and/or Poklemba; Lovinggood et al. does not cure these defects.

Based on at least the arguments contained herein, the rejection under 35 U.S.C. §103(a) of Claim 1 must be reversed.

2.B. The receiver of Claim 5 is patentable over Chalmers in view of Lovinggood et al., and further in view of Poklemba

Claim 5 recites a digital down-converter including a first mixer for converting a frequency of a received digital signal, sampled with a radio frequency (RF) or an intermediate frequency (IF), to a frequency of a first IF signal by multiplying the digital signal by a real signal, and a second mixer for converting the first IF signal converted by the first mixer to a second IF signal of a detection frequency for a detection process and then outputting the second IF signal as a complex signal by multiplying the first IF signal by a complex local signal; an RF unit for receiving an input signal and providing the received signal to the digital down-converter for frequency conversion; a filter for attenuating an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter, from an output of the radio receiver; and an analog-to-digital converter for sampling an output of the filter with a radio frequency or an intermediate frequency and providing the sampled signal to the digital down-converter; the second mixer further includes a first selector for cyclically selecting a multiplication value among cosine wave values of the local signal, and a second selector for cyclically selecting a multiplication value among sine wave values of the local signal.

2.B.1. The second mixer as recited in Claim 5 is not taught or disclosed by Chalmers

Claim 5 recites a second mixer for converting the first IF signal converted by the first mixer

to a second IF signal of a detection frequency for a detection process and then outputting the second IF signal as a complex signal by multiplying the first IF signal by a complex local signal. The Examiner equates this feature of Claim 5 with mixer 112 of Chalmers. The second mixer of Claim 5 receives the signal output from the first mixer. Chalmers in FIG. 1 illustrates its mixer 112 receiving a signal from amplifier 110.

Claim 5 further recites that the second mixer outputting the second IF signal as a complex signal by multiplying the first IF signal by a complex local signal. The Examiner now equates the second mixer of Claim 5 with mixer 132 illustrated in FIG. 1 of Chalmers. The Examiner has thus far equated the second mixer of Claim 5 with both mixer 112 and mixer 132 of FIG. 1 of Chalmers. Further, this feature of Claim 5 states that the second mixer multiplies the output of the first IF signal by a complex local signal. Neither mixer 112 nor mixer 132 of Chalmers multiplies the output of the decimation filter by a complex local signal.

The second mixer of Claim 5 is not taught or disclosed by Chalmers; Lovinggood et al. and/or Poklemba do not cure these defects.

2.B.2. The first and second selectors of Claim 5 are not taught or disclosed by Chalmers and/or Poklemba

Claim 5 still further recites that the second mixer comprises a first selector for cyclically selecting a multiplication value among cosine wave values of the local signal, and a second selector for cyclically selecting a multiplication value among sine wave values of the local signal. The Examiner opines that Poklemba discloses these features, and specifically points to the normal/inverting gating circuits (106 and 108) and multiplexer (110) of FIG. 4. The normal/inverting gating circuits 106 and 108 are not selectors as recited in Claim 5 and defined in the specification.

The first and second selectors of Claim 5 are not taught or disclosed by Chalmers and/or Poklemba; Lovinggood et al. does not cure these defects.

2.B.3. The filter for attenuating an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter of Claim 5 is distinguishable from the filter of Chalmers in view of Lovinggood et al., and further in view of Poklemba

In addition, Claim 5 recites a filter for attenuating an aliasing frequency component and an

image frequency component of the first mixer in the digital down-converter. This filter of Claim 5 is matched to the first mixer. The Examiner cites filter 102 of Chalmers as disclosing the filter for attenuating an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter of Claim 5. The filter 102 of Chalmers is a simple band pass filter as disclosed at col. 1, lines 20-21. The filter of Chalmers does not attenuate an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter.

The filter for attenuating an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter of Claim 5 are not taught or disclosed by Chalmers and/or Poklemba; Lovinggood et al. does not cure these defects.

Based on at least the arguments contained herein, the rejection under 35 U.S.C. §103(a) of Claim 5 must be reversed.

2.C. The digital down converter of Claim 16 is patentable over Chalmers in view of Lovinggood et al., and further in view of Poklemba

Claim 16 recites a digital down-converter for converting a frequency of a digital signal, received at a radio receiver and sampled with a radio frequency (RF) or an intermediated frequency (IF), to a detection frequency for a detection process, that includes a first mixer for converting and outputting a frequency of the received signal to a frequency of a first IF signal by multiplying the digital signal by a real signal; and a second mixer for dividing the frequency of the first IF signal into a cosine part and a sine part and processing the cosine part and the sine part with a polyphase structure for converting and decoding to the frequency of a second IF signal by multiplying the first IF signal by a complex local signal; the second mixer further includes a selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals.

2.C.1. The first mixer as recited in Claim 16 is not taught or disclosed by Chalmers

Claim 16 recites a first mixer for converting and outputting a frequency of the received signal to a frequency of a first IF signal by multiplying the digital signal by a real signal. The Examiner opines that the mixer 106 of Chalmers renders unpatentable this feature of Claim 16. The mixer 106

of Chalmers cited by the Examiner does not multiply the digital signal by a real signal. The mixer 106 of Chalmers multiplies an analog signal by a local oscillation signal.

The first mixer of Claim 16 is not taught or disclosed by Chalmers; Lovinggood et al. and/or Poklemba do not cure these defects.

2.C.2. The second mixer as recited in Claim 16 is not taught or disclosed by Chalmers

Claim 16 also recites a second mixer for dividing the frequency of the first IF signal into a cosine part and a sine part and processing the cosine part and the sine part with a polyphase structure for converting and decoding to the frequency of a second IF signal by multiplying the first IF signal by a complex local signal. The Examiner cites mixer 112 of Chalmers as disclosing these features. The mixer 112 of Chalmers does not divide any frequency into a cosine part and a sine part, nor does mixer 112 multiply the first IF signal by a complex local signal. Chalmers in FIG. 1 illustrates its mixer 112 receiving a signal from amplifier 110.

Claim 16 further recites that the second mixer outputting the second IF signal by multiplying the output of the first IF signal by a complex local signal. The Examiner now equates the second mixer of Claim 16 with mixer 132 illustrated in FIG. 1 of Chalmers. The Examiner has thus far equated the second mixer of Claim 1 with both mixer 112 and mixer 132 of FIG. 1 of Chalmers. Further, this feature of Claim 16 states that the second mixer multiplies the first IF signal by a complex local signal. Neither mixer 112 nor mixer 132 of Chalmers multiplies the output of the decimation filter by a complex local signal.

The second mixer of Claim 16 is not taught or disclosed by Chalmers; Lovinggood et al. and/or Poklemba do not cure these defects.

2.C.3. The selector of Claim 16 is not taught or disclosed by Chalmers and/or Poklemba

Claim 16 still further recites that the second mixer comprises a selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals. The Examiner opines that Poklemba discloses these features, and specifically points to the normal/inverting gating circuits (106 and 108) and multiplexer (110) of FIG. 4. The normal/inverting gating circuits 106 and 108 of Poklemba are two selectors; Claim 16 recites one

selector. The normal/inverting gating circuits 106 and 108 of Poklemba are two selectors; Claim 16 recites one selector.

The normal/inverting gating circuits 106 and 108 of Poklemba is not the selector as recited in Claim 16 and defined in the specification.

The selector of Claim 16 is not taught or disclosed by Chalmers and/or Poklemba; Lovinggood et al. does not cure these defects.

2.C.4. The selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals of Claim 16 is distinguishable from the filter and gating circuits of Chalmers in view of Lovinggood et al., and further in view of Poklemba

Claim 16 still further recites a selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals. The Examiner opines that the filters of FIG. 7 of Chalmers and the normal/inverting gating circuits of Poklemba. The filters of Chalmers are a series chain of FIR filters; Poklemba merely recites the normal/inverting gating circuits (106 and 108) and multiplexer (110) of FIG. 4 and that the NORM/INVERT (106, 108) outputs (+1, 0, -1, 0) of the cosine sample and (0, +1, 0, -1) of the sine sample. This combination in no way teaches or discloses a selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals as recited in Claim 16.

The selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals of Claim 16 is not taught or disclosed by Chalmers and/or Poklemba; Lovinggood et al. does not cure these defects.

2.C.5. The selector of Claim 16 has never been rejected

Finally, the Examiner rejects on page 7 of the June 2006 Office Action a first selector and a second selector allegedly recited in Claim 16. It is apparent that the Examiner merely copied the previous rejections. Claim 16 recites that the second mixer includes a selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals. These features of Claim 16 have never been addressed and therefore never properly rejected by the Examiner. Although these examination errors were presented to the Examiner during a telephonic interview conducted on July 26, 2006, and again raised in the Applicants' Response of

November 17, 2006, these fatal defects have yet to be properly addressed.

Based on at least the arguments contained herein, the rejection under 35 U.S.C. §103(a) of Claim 16 must be reversed.

2.D. Claims 1, 5 and 16 are patentable over Chalmers in view of Lovinggood et al., and further in view of Poklemba

Based on at least the foregoing, and as the Examiner has failed to make out a prima facie case for an obviousness rejection, the rejection of Claims 1, 5 and 16 must be reversed.

It is well settled that in order for a rejection under 35 U.S.C. §103(a) to be appropriate, the claimed invention must be shown to be obvious in view of the prior art as a whole. A claim may be found to be obvious if it is first shown that all of the recitations of a claim are taught in the prior art or are suggested by the prior art. In re Royka, 490 F.2d 981, 985, 180 U.S.P.Q. 580, 583 (C.C.P.A. 1974), cited in M.P.E.P. §2143.03.

The Examiner has failed to show that all of the recitations of Claims 1, 5 and 16 are taught or suggested by either Chalmers, Lovinggood et al., or Poklemba, or the combination thereof. Accordingly, the Examiner has failed to make out a prima facie case for an obviousness rejection.

Independent Claims 1, 5 and 16 are not rendered unpatentable by Chalmers, Lovinggood et al., or Poklemba, or the combination thereof. Thus, independent Claims 1, 5 and 16 are allowable.

3. Dependent Claims 2-4, 6-15, 17 and 18 are not unpatentable over Chalmers in view of Lovinggood et al., in view of Poklemba, and further in view of Ostman

Dependent Claims 2-4, 6-15, 17 and 18 were said to be unpatentable over Chalmers in view of Lovinggood et al., in view of Poklemba, and further in view of Ostman. Without conceding the patentability per se of dependent Claims 2-4, 6-15, 17 and 18, these are likewise believed to be allowable by virtue of their dependence on their respective independent claims.

## CONCLUSION

Based on at least the foregoing, and as the Examiner has failed to make out a prima facie case for an obviousness rejection, the rejection of Claims 1-18 must be reversed.

It is well settled that in order for a rejection under 35 U.S.C. §103(a) to be appropriate, the claimed invention must be shown to be obvious in view of the prior art as a whole. A claim may be found to be obvious if it is first shown that all of the recitations of a claim are taught in the prior art or are suggested by the prior art. In re Royka, 490 F.2d 981, 985, 180 U.S.P.Q. 580, 583 (C.C.P.A. 1974), cited in M.P.E.P. §2143.03.

The Examiner has failed to show that all of the recitations of Claims 1, 5 an d16 are taught or suggested by either Chalmers, Lovinggood et al., or Poklemba, or the combination thereof. Accordingly, the Examiner has failed to make out a prima facie case for an obviousness rejection.

Independent Claims 1, 5 and 16 are not rendered unpatentable by Chalmers, Lovinggood et al., or Poklemba, or the combination thereof. Thus, independent Claims 1, 5 and 16 are allowable.

Accordingly, dependent Claim 2-4, 6-15, 17 and 18 are allowable because of their dependence upon independent Claim 1, 5 and 16.

Dated: December 26, 2006

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## CLAIMS APPENDIX

1. (Previously Presented) A digital down-converter for converting a frequency of a digital signal, received at a radio receiver and sampled with a radio frequency (RF) or an intermediate frequency (IF), to a detection frequency for a detection process, comprising:

a first mixer for converting and outputting a frequency of the digital signal to a frequency of a first IF signal by multiplying the digital signal by a real signal;

a decimation filter for suppressing unwanted components among the frequency of the first IF signal from the first mixer; and

a second mixer for converting the frequency of the first IF signal having only wanted components outputted by the decimation filter to a second IF signal of the detection frequency, and outputting the second IF signal as a complex signal by multiplying the output of the decimation filter by a complex local signal, the second mixer comprising:

a first selector for cyclically selecting a multiplication value among cosine wave values of the local signal; and

a second selector for cyclically selecting a multiplication value among sine wave values of the local signal.

2. (Original) The digital down-converter as claimed in claim 1, wherein a frequency of the first IF signal is 1/4 a sampling frequency.

3. (Previously Presented) The digital down-converter as claimed in claim 2, further comprising an automatic gain control (AGC) amplifier for amplifying an output of the decimation filter and inputting the amplified output to the second mixer.

4. (Previously Presented) The digital down-converter as claimed in claim 2, wherein the second mixer further comprises a multiplier for multiplying the output of the decimation filter by a certain ratio of a sampling frequency and a decoding means for decoding the multiplied signal through the multiplier.

5. (Previously Presented) A receiver comprising:

a digital down-converter including a first mixer for converting a frequency of a received digital signal, sampled with a radio frequency (RF) or an intermediate frequency (IF), to a frequency of a first IF signal by multiplying the digital signal by a real signal, and a second mixer for converting the first IF signal converted by the first mixer to a second IF signal of a detection frequency for a detection process and then outputting the second IF signal as a complex signal by multiplying the first IF signal by a complex local signal;

an RF unit for receiving an input signal and providing the received signal to the digital down-converter for frequency conversion;

a filter for attenuating an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter, from an output of the radio receiver; and

an analog-to-digital converter for sampling an output of the filter with a radio frequency or an intermediate frequency and providing the sampled signal to the digital down-converter;

wherein the second mixer further comprises:

a first selector for cyclically selecting a multiplication value among cosine wave values of the local signal; and

a second selector for cyclically selecting a multiplication value among sine wave values of the local signal.

6. (Original) The receiver as claimed in claim 5, wherein a frequency of the first IF signal is 1/4 a sampling frequency.

7. (Previously Presented) The receiver as claimed in claim 6, further comprising an automatic gain control (AGC) amplifier for amplifying an output of the first mixer of the digital down-converter, and

wherein the first and second selectors are connected to the output of the AGC.

8. (Previously Presented) The receiver as claimed in claim 6, wherein the second mixer of the digital down-converter is constructed in a polyphase structure comprised of a decimation filter and a quadrature converter, and

wherein the first and second selectors are connected to the output of the decimation filter.

9. (Previously Presented) The digital down-converter as claimed in Claim 3, the second mixer further comprises:

a multiplier for multiplying the output of the automatic gain control (AGC) by a certain ratio of a sampling frequency and a decoding means for decoding the multiplied signal through the multiplier.

10. (Previously Presented) The digital down-converter as claimed in Claim 2, wherein the first and second selectors are connected to the output of the decimation filter.

11. (Previously Presented) The digital down-converter as claimed in Claim 3, wherein the first and second selectors are connected to the output of the AGC.

12. (Previously Presented) The digital down-converter as claimed in Claim 10, wherein the first selector has multiplication values among cosine wave values as 1, 0, -1 and 0, outputs a multiplication result corresponding to a multiplication value '1', outputs a multiplication result corresponding to '-1' by inversion, and a multiplication result '0' corresponding to a multiplication value '0'.

13. (Previously Presented) The digital down-converter as claimed in Claim 11, wherein the first selector has multiplication values among cosine wave values as 1, 0, -1 and 0, outputs a multiplication result corresponding to a multiplication value '1', outputs a multiplication result corresponding to '-1' by inversion, and a multiplication result '0' corresponding to a multiplication value '0'.

14. (Previously Presented) The digital down-converter as claimed in Claim 10, wherein the second selector has multiplication values among sine wave values as 1, 0, -1 and 0, outputs a multiplication result corresponding to a multiplication value '1', outputs a multiplication result corresponding to '-1' by inversion, and a multiplication result '0' corresponding to a multiplication

value '0'.

15. (Previously Presented) The digital down-converter as claimed in Claim 10, wherein the second selector has multiplication values among sine wave values as 1, 0, -1 and 0, outputs a multiplication result corresponding to a multiplication value '1', outputs a multiplication result corresponding to '-1' by inversion, and a multiplication result '0' corresponding to a multiplication value '0'.

16. (Previously Presented) A digital down-converter for converting a frequency of a digital signal, received at a radio receiver and sampled with a radio frequency (RF) or an intermediated frequency (IF), to a detection frequency for a detection process, comprising:

a first mixer for converting and outputting a frequency of the received signal to a frequency of a first IF signal by multiplying the digital signal by a real signal; and

a second mixer for dividing the frequency of the first IF signal into a cosine part and a sine part and processing the cosine part and the sine part with a polyphase structure for converting and decoding to the frequency of a second IF signal by multiplying the first IF signal by a complex local signal, the second mixer comprising:

a selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals.

17. (Previously Presented) The digital down-converter as claimed in Claim 16, wherein a frequency of the first IF signal is ¼ a sampling frequency.

18. (Previously Presented) The digital down-converter as claimed in Claim 17, further comprising an automatic gain control (AGC) amplifier for amplifying ~~of~~ the output of the first mixer and inputting the amplified output to the cosine part and the sine part of the second mixer.

19. (Cancelled)

## EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. 1.130, 1.131, 1.132 or entered by the Examiner and relied upon by Appellant.

## RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 C.F.R. 41.37.